changes in the link quality. Low-overhead continuous request and grant channels that are consistent with the framework and are suitable to manage QoS for services with maximum delay requirements of less than 100 ms. A process is disclosed for computing T/P requirements for different levels of congestion by using a drop priority for packets. A compact encoding of the rate request channel is disclosed that provides the BS resource manager information to determine level of congestion at the packet queues distributed among the MS. Further, it allows the BS resource manager to make intelligent allocation decisions among the contending MS. Therefore, the BS resource manager operates to allocate the resource among the contending MS, including operation of the closed loop rate control in soft handoff.

Various aspects of the invention may be more apparent by referring to various steps depicted in FIG. **4**. FIG. **4** depicts a flow **400** of messages and processing steps at a BS and a MS in the communication system **100**. The receiver and transmitter systems **200** and **300** shown in FIGS. **2** and **3** may operate to perform various steps when incorporated in a respective base station or mobile station in the communication system **100**. At step **401**, the mobile station determines packets of data for transmission for a number of communication services. At steps **402** and **403**, respectively, the mobile station determines a transmission deadline of each of the packets of data and arranges the packets of data in a queue for transmission in accordance with the determined transmission deadline. At steps **405**, **406** and **407**, respectively, the mobile station determines a data rate for transmission of the packets of data based on the arrangement of the packets of data in the queue allowing for meeting the transmission deadline for each of the packets of data, determines duration of the determined data rate for transmissions of the packets of data based on the arrangement of the packets of data in said queue, and communicates the data rate and the duration from the mobile station to the base station. At step **408**, the base station determines whether available resources allow for allocation at the base station for transmission from the mobile station at the determined data rate and duration. At step **409**, the base station communicates acceptance of the determined data rate for transmission of the packets of data from the mobile station. At step **410**, the mobile station transmits at the accepted data rate. At step **411**, the base station may indicate a congestion level alert to the mobile station that the determined available resources disallow for allocation at the base station for transmission from the mobile station at the determined data rate. At steps **412**, **413** and **414**, the mobile station drops at least a packet of data of the packets of data in the queue to determine a new queue of packets of data, determines a new data rate for transmission of the new queue of packets of data, the new data rate being lower than the previously determined data rate, and determines a new duration for use of the determined new data rate for transmissions of the packets of data based on the arrangement of the packets of data in the new queue. The flow **400** moves to step **408** to repeat the determination for acceptance or rejection.

Those of skill in the art would further appreciate that the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present invention.

The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein may be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general-purpose processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

The steps of a method or algorithm described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination. A software module may reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. An exemplary storage medium is coupled to the processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC. The ASIC may reside in a user terminal. In the alternative, the processor and the storage medium may reside as discrete components in a user terminal.

The previous description of the preferred embodiments is provided to enable any person skilled in the art to make or use the present invention. The various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the inventive faculty. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

The invention claimed is:

1. In a communication system, a method for determining a data rate for reverse link communication from a mobile station to a base station, the method comprising:

determining, at said mobile station, packets of data for transmission from the mobile station for a number of communication services;

determining, at said mobile station, a transmission deadline of each of said packets of data;

arranging, at said mobile station, the packets of data in a queue for transmission in accordance with said determined transmission deadline;

determining, at said mobile station, a data rate for transmission of the packets of data based on the arrangement of said packets of data in said queue allowing for meeting the transmission deadline for each of said packets of data;